



Poechmueller

Attorney Docket: INTECH 3.0-102 03 P 51716

Filed:

September 12, 2003

Examiner:

TBD

Serial No.:

10/661,295

Art Unit:

2812

For:

Automated Layout Transformation System and Method

Mail Stop: Amendment Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08B that may be considered material to the examination of the above-identified application. A copy of the PCT International Search Report regarding the references filed is included for your convenience.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Respectfully submitted,

April 28, 2005

Date

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Date of Deposit:

April 28, 2005

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Information Disclosure Statement (1 page)
IDS Form PTO/SB/08B with four (4) references cited (1 page)
Copy of four (4) cited references
PCT International Search Report (3 pages)
Return Postcard

Respectfully submitted

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PTO/SB/08b (08-03)

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Substitute for form 1449B/PTO Complete if Known **Application Number** 10/661,295 INFORMATION DISCLOSURE Filing Date 9/12/2003 STATEMENT BY APPLICANT First Named Inventor Poechmueller Art Unit 2812 Examiner Name (Use as many sheets as necessary) TBD Sheet Attorney Docket Number INTECH 3.0-102 03 P 51716

		NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²		
	1	ALLAN, G., et al., "An Yield Improvement Technique for IC Layout Using Local Design Rules," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, November 11, 1992, pp. 1355-1362, Vol. 11, No. 11.			
	2	BAMJI, C., et al., "Enhanced Network Flow Algorithm for Yield Optimization," Proc Des Autom Conf; Proceedings - Design Automation Conference, June 3, 1996, pp. 746-751.			
	3	MALY, W., et al., "Design for Manufacturability in Submicron Domain," Computer-Aided Design, IEEE/ACM International Conference on San Jose, CA, November 10-14, 1996, pp. 690-697.			
	4	CHOTIN, E., et al., "A Design Planner Including a Fast Predictive Floorplanning Tool," Euro ASIC '90, May 29, 1990, pp. 208-213, Paris, France.			
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Examiner	Date
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Signature	Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 'Applicant's unique citation designation number (optional). 'Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.